interposed therebetween and said second semiconductor island does not overlap any portion of the conductive film;

forming a pair of first N-type impurity regions in the first semiconductor island with a channel region therebetween;

forming at least one second N-type impurity region between the channel region and the first N-type impurity regions wherein a concentration of an N-type impurity in the second N-type impurity region is lower than that in said first N-type impurity regions;

forming a pair of P-type impurity regions in the second semiconductor island with a channel region therebetween;

forming a second insulating film over said first and second semiconductor islands;

forming a second gate electrode over the channel region of the first semiconductor island and a third gate electrode over the channel region of the second semiconductor island,

wherein there is an overlap between the first gate electrode and the second N-type impurity region of the first semiconductor island and there is no overlap between the second gate electrode and the second N-type impurity region.

34. The method according to claim 33 wherein said conductive film comprises a material selected from the group consisting of Ta, Cr, Ti, W, Mo and Is.

35. The method according to claim 33 wherein said second and third gate electrodes are formed by patterning a conductive layer, said conductive layer comprising a material selected from the group consisting of tantalum, chromium, titanium, tungsten, molybdenum, and silicon.

36. A method of manufacturing a semiconductor device comprising:

forming a conductive film over a substrate;

patterning said conductive film to form at least one first wiring, said first wiring including at least one first gate electrode;

forming a first insulating film over said first wiring and said substrate;

forming a first semiconductor island and a second semiconductor island wherein said first semiconductor island is located over said first gate electrode with said first insulating film interposed therebetween and said second semiconductor island does not overlap any portion of the conductive film;

forming a pair of first N-type impurity regions in the first semiconductor island with a channel region therebetween;

forming at least one second N-type impurity region between the channel region and the first N-type impurity regions wherein a concentration of an N-type impurity in the second N-type impurity region is lower than that in said first N-type impurity regions;

forming a pair of P-type impurity regions in the second semiconductor island with a channel region therebetween;

forming a second insulating film over said first and second semiconductor islands;

forming a second gate electrode over the channel region of the first semiconductor island and a third gate electrode over the channel region of the second semiconductor island,

wherein there is an overlap between the first gate electrode and the second N-type impurity region of the first semiconductor island and there is no overlap between the second gate electrode and the second N-type impurity region, and

wherein the first gate electrode is electrically connected to the second gate electrode.

37. The method according to claim 36 wherein said conductive film comprises a material selected from the group consisting of Ta, Cr, Ti, W, Mo and Is.

38. The method according to claim 36 wherein said second and third gate electrodes are

formed by patterning a conductive layer, said conductive layer comprising a material selected from the group consisting of tantalum, chromium, titanium, tungsten, molybdenum, and silicon.

39. A method of manufacturing a semiconductor device comprising:

forming a conductive film over a substrate;

patterning said conductive film to form at least one first wiring, said first wiring including at least one first gate electrode;

forming a first insulating film over said first wiring and said substrate;

forming a first semiconductor island and a second semiconductor island wherein said first semiconductor island is located over said first gate electrode with said first insulating film interposed therebetween and said second semiconductor island does not overlap any portion of the conductive film;

forming a pair of first N-type impurity regions in the first semiconductor island with a channel region therebetween;

forming at least one second N-type impurity region between the channel region and the first N-type impurity regions wherein a concentration of an N-type impurity in the second N-type impurity region is lower than that in said first N-type impurity regions;

forming a pair of P-type impurity regions in the second semiconductor island with a channel region therebetween;

forming a second insulating film over said first and second semiconductor islands;

forming a second gate electrode over the channel region of the first semiconductor island and a third gate electrode over the channel region of the second semiconductor island,

wherein the first gate electrode extends beyond both side edges of the second gate electrode.

40. The method according to claim 39 wherein said conductive film comprises a material selected from the group consisting of Ta, Cr, Ti, W, Mo and Is.

41. The method according to claim 39 wherein said second and third gate electrodes are formed by patterning a conductive layer, said conductive layer comprising a material selected from the group consisting of tantalum, chromium, titanium, tungsten, molybdenum, and silicon.

42. A method of manufacturing a semiconductor device comprising:

forming a conductive film over a substrate;

patterning said conductive film to form at least one first wiring, said first wiring including at least one first gate electrode;

forming a first insulating film over said first wiring and said substrate;

forming a first semiconductor island and a second semiconductor island wherein said first semiconductor island is located over said first gate electrode with said first insulating film interposed therebetween and said second semiconductor island does not overlap any portion of the conductive film;

forming a pair of first N-type impurity regions in the first semiconductor island with a channel region therebetween;

forming at least one second N-type impurity region between the channel region and the first N-type impurity regions wherein a concentration of an N-type impurity in the second N-type impurity region is lower than that in said first N-type impurity regions;

forming a pair of P-type impurity regions in the second semiconductor island with a channel region therebetween;

forming a second insulating film over said first and second semiconductor islands;

forming a second gate electrode over the channel region of the first semiconductor island and a third gate electrode over the channel region of the second semiconductor island;

forming a third insulating film over the second and third gate electrodes; and

forming a pixel electrode over the third insulating film,

wherein the first gate electrode is electrically floating, and

wherein the first gate electrode extends beyond both side edges of the second gate electrode.

43. The method according to claim 42 wherein said conductive film comprises a material selected from the group consisting of Ta, Cr, Ti, W, Mo and Is.

44. The method according to claim 42 wherein said second and third gate electrodes are formed by patterning a conductive layer, said conductive layer comprising a material selected from the group consisting of tantalum, chromium, titanium, tungsten, molybdenum, and silicon.

45. A method of manufacturing a semiconductor device comprising:

forming a conductive film over a substrate;

patterning said conductive film to form at least one first wiring, said first wiring including at least one first gate electrode;

forming a first insulating film over said first wiring and said substrate;

forming a first semiconductor island and a second semiconductor island wherein said first semiconductor island is located over said first gate electrode with said first insulating film interposed therebetween and said second semiconductor island does not overlap any portion of the conductive film;

forming a pair of first N-type impurity regions in the first semiconductor island with a channel region therebetween;

forming at least one second N-type impurity region between the channel region and the first N-type impurity regions wherein a concentration of an N-type impurity in the second N-

type impurity region is lower than that in said first N-type impurity regions;

forming a pair of P-type impurity regions in the second semiconductor island with a channel region therebetween;

forming a second insulating film over said first and second semiconductor islands;

forming a second gate electrode over the channel region of the first semiconductor island and a third gate electrode over the channel region of the second semiconductor island,

wherein the first gate electrode extends beyond both side edges of the second gate electrode and is connected to a fixed potential.

46. The method according to claim 45 wherein said conductive film comprises a material selected from the group consisting of Ta, Cr, Ti, W, Mo and Is.

47. The method according to claim 45 wherein said second and third gate electrodes are formed by patterning a conductive layer, said conductive layer comprising a material selected from the group consisting of tantalum, chromium, titanium, tungsten, molybdenum, and silicon.

48. A method of manufacturing a semiconductor device comprising:

forming a first conductive film over a substrate;

patterning said first conductive film to form at least one first wiring, said first wiring including at least one first gate electrode;

forming a first insulating film over said first wiring and said substrate;

forming a first semiconductor island and a second semiconductor island wherein said first semiconductor island is located over said first gate electrode with said first insulating film interposed therebetween and said second semiconductor island does not overlap any portion of the conductive film;

forming a second insulating film over said first and second semiconductor islands;

forming a second conductive film over the second insulating film;

etching a portion of the second conductive film to form a second gate electrode over the first semiconductor island while a portion of the conductive film over the second semiconductor island is not etched wherein said first gate electrode extends beyond side edges of the second gate electrode;

introducing an N-type impurity into the first semiconductor island at a first concentration in accordance with a pattern of the second gate electrode wherein said N-type impurity region is prevented from being introduced into the second semiconductor island during the first introduction of the N-type impurity;

etching another portion of the conductive film to form a third gate electrode over the second semiconductor island after the introduction of the N-type impurity;

introducing a P-type impurity into the second semiconductor island in accordance with a pattern of the third gate electrode wherein said P-type impurity is prevented from being introduced into the first semiconductor island during the introduction of said P-type impurity;

forming a first resist mask and a second resist mask wherein said first resist mask covers the second gate electrode and extends beyond side edges of the second gate electrode, and said second resist mask is formed over the third gate electrode;

introducing an N-type impurity into the first semiconductor island in accordance with said first resist mask at a second concentration greater than the first concentration.

49. The method according to claim 39 wherein said conductive film comprises a material selected from the group consisting of Ta, Cr, Ti, W, Mo and Is.